In the Claims:

1. (Previously Presented) A method of manufacturing a module, the method comprising:

providing a device that includes a connection area extending over a top surface of the device, wherein the connection area comprises a compliant 3D structure that includes a conductor overlying a compliant base element, the conductor being integral with a redistribution layer that overlies the device;

applying a casting compound over the top surface of the device;

after applying a casting compound, reducing a thickness of the casting compound so that the connection area protrudes through the casting compound.

2. (Currently Amended) The method of claim 1 further comprising, after applying the casting compound, mounting the module to a [[the]] printed circuit board.

3. (Currently Amended) The method of claim 1 further comprising, after forming the casting compound, attaching the module to a [[the]] lead frame.

4. (Previously Presented) The method of claim 26 wherein electrically coupling the connection area comprises soldering the connection area to the terminal.

5. (Canceled)

6. (Canceled)

7. (Original) The method of claim 1 wherein the device comprises a semiconductor wafer.

8. (Original) The method of claim 7 and further comprising separating the wafer into a plurality of individual chips, wherein the casting compound is applied to the wafer before the separating.

9. (Original) The method of claim 8 wherein separation corridors between the chips on the wafer are exposed before the separating.

10. (Original) The method of claim 9 wherein the separation corridors are exposed by a photolithographic process.

11. (Original) The method of claim 9 wherein the separation corridors are exposed with use of a laser beam.

12. (Currently Amended) The method of claim 8 wherein the [[wafer]] casting compound is cooled ~~to a temperature at which the casting compound is adequately brittle~~ before separating the wafer into a plurality of individual chips.

13. (Original) The method of claim 1 wherein the casting compound is applied uniformly by spraying, dispensing or printing.

14. (Original) The method of claim 1 wherein the casting compound has thermal and mechanical properties comparable to those of silicon.

15. (Original) The method of claim 14 wherein the casting compound comprises a silicon-based material.

16. (Original) The method of claim 14 wherein the casting compound comprises a thermoplastic material.

17. (Original) The method of claim 14 wherein the casting compound comprises an epoxy resin.

18. (Canceled)

19. (Previously Presented) The method of claim 1 wherein the thickness of the casting compound is reduced by thermal removal.

20. (Previously Presented) The method of claim 1 wherein the thickness of the casting compound is reduced by etching.

21. (Previously Presented) A method for improving the mechanical properties of a BOC module arrangement in which chips have 3D structures which are mechanically and electrically connected by means of solder connections to terminal contacts on a printed circuit board or leadframe, the method characterized in that a casting compound is applied over a top surface of the chips, and excess thickness of the casting compound is removed, in such a way that tips of the 3D structures protrude from the compound, wherein the 3D structures comprise compliant 3D structures each of which includes a conductor overlying a compliant base element, the conductor being integral with a redistribution layer that overlies the top surface of the chips.

22. (Canceled)

23. (Previously Presented) The method of claim 21 wherein the conductor comprises metal.

24. (Original) The method of claim 21 wherein the chips comprise a plurality of chips on a semiconductor wafer.

25. (Original) The method of claim 21 wherein the chips comprise individual semiconductor dies.

26. (Previously Presented) The method of claim 1, further comprising, after applying a casting compound, electrically coupling the connection area to a terminal of a second apparatus.

27. (Previously Presented) The method of claim 8, wherein separating the wafer into a plurality of individual chips comprises using a laser to separate the wafer.